Detector Support Group
Weekly Report, 2019-07-31

Summary

Hall A – BigBite ECAL

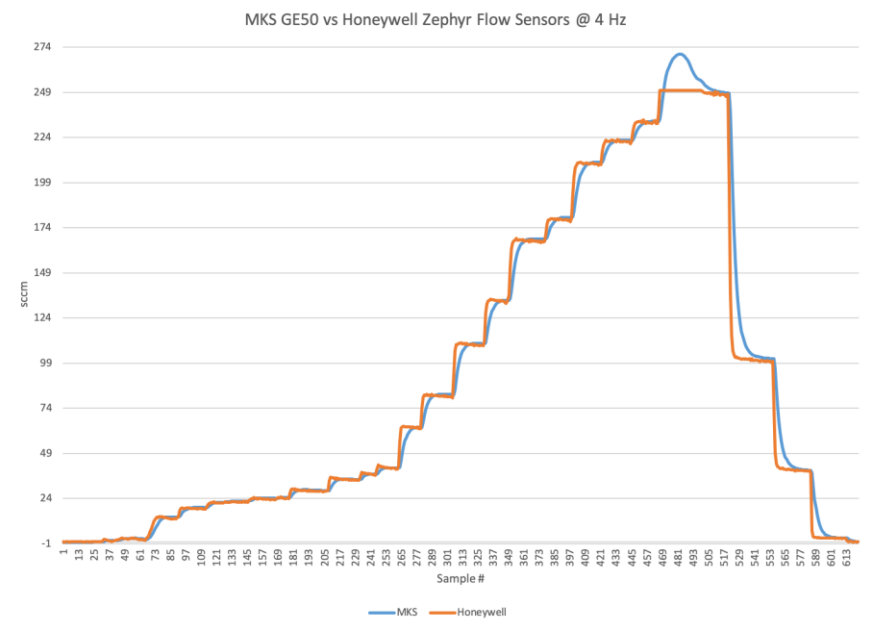
- Cut 30 foil rectangles and wrapped 27 light guides.

Hall A – BigBite HCAL

- Terminated BNC end of eight BNC-to-LEMO cables.
- Stripped 18 cables.

Hall A – GEM Gas System

- Tested SMC 586 series plastic needle valve, finding that there is very little adjustment available between zero and full flow.
  - ✶ Legris 7770 series plastic needle valve has been ordered to evaluate as an alternative.
- Using pump and manual valve, compared MKS GE50 mass flow controller with Honeywell Zephyr flow sensor.



Data from comparison of Honeywell Zephyr (orange) and MKS GE50 (blue).

Hall B – Magnets

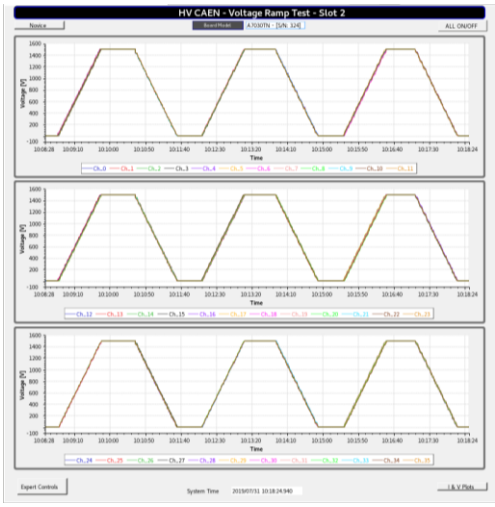
- Tested FastDAQ cRIO using DAQmx API in place of FPGA.
  - ✶ Initial test resulted in less overlap and missed samples compared to FPGA.
  - ✶ Modified code to write PVs in a forced order to see if forcing a sequence resolved overlapping/missing samples issue; results inconclusive.
- Tested lower 2 kHz data rate with DAQmx.

Hall C – EPICS

- Added runtime counter to PLC to indicate duration PLC has been running in EtherIP test.
- Added runtime counter to IOC to indicate duration IOC has been running in EtherIP test.

Hall C – CAEN HV Test Station

- Developed CSS-BOY screen to test voltage ramp up/down of CAEN-A7030TN modules that plots all 36 channels' voltage vs time.



CSS-BOY screen displaying voltages for 36 channels during test.

- During tests of three A7030TN modules, found that inconsistencies previously seen between EPICS PV set value and the mainframe's internal set value persisted, causing channels to fail tests.
  - ✶ Different CAEN mainframe provided to allow tests to continue.
- Completed design of HV multiplexer that uses LV relays to control four banks of 12 HV relays, reducing the amount of control channels necessary to actuate 48 HV relays.

Hall D – WEDM

- Used newly added Boolean array PVs to add byte monitors to Solenoid power supply WEDM screen for power supply status bits.
- Added EDM calculation PVs to Solenoid voltage tap screen using for coil voltage sums.

DSG R&D – cRIO Test Stand

- Prepared NI-9870 serial module for testing.

DSG R&D – LV Chassis FPGA

- Installed and set up Quartus II software for Altera FPGA-SOC board.
- Completed example FPGA program to verify correct installation of software.

Accelerator Division R&D

- Adjustments made to bonding parameters for superconducting Nb_3Sn strip resonator sample, allowing 6 of 20 bonds to be completed.

Engineering Division R&D

- Completed four BPM PCBs
- Soldered three IC FPGAs.